

D1  
portion of data and the second portion of data are included in the same packet].

D2  
9 8  
159. (Amended) The method of claim 158 wherein the write request is included in a first packet, and the first portion of data and the second portion of data are included in a second packet.

10 8  
160. (Amended) The method of claim 158 wherein the write request includes an operation code[, the first portion of data and the second portion of data are included in the same packet].

[ Kindly ADD the following claims:

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1 -- 176. A method of controlling a synchronous memory device,  
2 wherein the memory device includes a plurality of memory cells, the  
3 method of controlling the memory device comprises:  
4 providing first block size information to the memory device,  
5 wherein the first block size information defines an amount of data to  
6 be input by the memory device in response to a write request;  
7 issuing the write request to the memory device, wherein the memory  
8 device samples the write request synchronously with respect to an  
9 external clock and, in response to the write request, the memory device  
10 samples first and second portions of data;  
11 providing a first portion of data to the memory device  
12 synchronously with respect to a rising edge transition of an external  
13 clock signal; and

14 providing a second portion of data to the memory device  
15 synchronously with respect to a falling edge transition of the external  
16 clock signal.

1 <sup>27</sup>  
<sup>26</sup>  
177. The method of claim 176 wherein the write request is included  
2 in a first packet and both the first and second portions of data are  
3 included in a second packet.

1 <sup>28</sup>  
<sup>26</sup>  
178. The method of claim 176 wherein the write request includes  
2 an operation code.

1 <sup>29</sup>  
<sup>28</sup>  
179. The method of claim 178 wherein the memory device samples the  
2 operation code synchronously with respect to a first transition of the  
3 external clock signal.

1 <sup>30</sup>  
<sup>26</sup>  
180. The method of claim 176 wherein:  
2 a first portion of the amount of data is sampled by the  
3 memory device in response to a rising edge transition of the  
4 external clock signal; and  
5 a second portion of the amount of data is sampled by  
6 the memory device in response to a falling edge transition  
7 of the external clock signal.

1 <sup>31</sup>  
<sup>26</sup>  
181. The method of claim 176 wherein the first block size  
2 information and the write request are included in a packet.

1 <sup>32</sup>  
<sup>26</sup>  
182. The method of claim 176 further including:

2 providing second block size information to the memory device,  
3 wherein the second block size information defines an amount of data to  
4 be output by the memory device in response to a read request;  
5 issuing a first read request to the memory device; and  
6 receiving the amount of data output by the memory device.

33 26  
1 183. The method of claim 176 further including providing access  
2 time information to the memory device, wherein the access time  
3 information is representative of a number of clock cycles of the  
4 external clock signal to transpire before the memory device outputs  
5 data.

34 26  
1 184. The method of claim 176 further including providing the  
2 external clock signal to the memory device wherein:  
3 in response to a first edge transition of the external clock  
4 signal the memory device samples the first portion of the data;  
5 and  
6 in response to a second edge transition of the external  
7 clock signal the memory device samples the second portion of the  
8 data, wherein the first and second edge transitions are from the  
9 same clock cycle of the external clock signal.

35 26  
1 185. The method of claim 176 wherein the external clock signal is  
2 provided by an external clock generator.